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EXAMINER	
TRAN, TRANG U	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,006	KIM ET AL.	
	Examiner	Art Unit	
	Trang U. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *2,3,8,9,19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,10-18 and 21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/30/04; 11/03/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species IV, claims 1, 4-7, 10-18 and 21-28 (Figs. 8 and 9A-9P) in the reply filed on April 25, 2007 is acknowledged. The traversal is on the ground(s) that claim 1 is generic to all of Species, that the Examiner would not be unduly burdened if forced to examiner Species I-IV, and that Election of Species Requirement is improper because Figs. 6 and 8 are subcomponents of the larger conversion apparatus of Fig. 1 but not species. This is not found persuasive because it is a serious burden on the Examiner if a restriction is not required because the search for at least different species Figs. 3-9 is a serious burden on the Examiner. It is agreed that claim 1 is generic to Species I-IV. After reconsideration, it is found that there are four Species disclosed in this specification: Species I : Figs. 3 and 4A-4F, Species II: Fig. 5, Species III: Figs. 6 and 7A-7O, and Species IV: Figs. 8-9P.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 2-3, 8-9, 19-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected claims, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on April 25, 2007.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 16-18, 21-25 and 28 rejected under 35 U.S.C. 102(b) as being anticipate by Peterson et al. (US Patent No. 4,386,367).

In considering claim 16, Peterson et al discloses all the claimed subject matter, note 1) the claimed a counter generating count values at a progressive scanning frequency such that the count values are associated with a period of progressive scan data is met by the write counter 50 and the line counter 70 (Fig. 3, col. 4, lines 5-43), 2) the claimed a memory is met by the storage device 36 (Fig. 3, col. 4, line 5 to col. 5, line 26), 3) the claimed a write address generator generating write addresses for writing progressive scan data into the memory based on output of the counter is met by the write address control circuit 52 and the write counter 50 (Figs. 3 and 4, col. 4, line 5 to col. 6, line 48), and 4) the claimed a read address generator generating read addresses for outputting the progressive scan data written into the memory as interlaced scan data is met by the read address control circuit 56 and the read counter 54 (Figs. 3 and 4, col. 4, line 5 to col. 6, line 48).

In considering claim 17, the claimed wherein the second converter further comprises: an address controller selectively applying the write and read addresses to the memory from the write and read address generators is met by the address MUX 58 which is switching alternately between the write address and the read address (Figs. 3 and 4, col. 4, line 5 to col. 6, line 48).

In considering claim 18, the claimed wherein the address controller controls the application of the write and read addresses to the memory such that a scan line of interlaced scan data is read from the memory while progressive scan data for the scan line is written to the memory is met by the address MUX 58 which is switching alternately between the write address and the read address (Figs. 3 and 4, col. 4, line 5 to col. 6, line 48).

In considering claim 21, the claimed wherein the counter generates count values associated with two consecutive scan lines of progressive scan data is met by the line counter 70 (Fig. 3, col. 4, lines 5-43).

In considering claim 22, Peterson et al discloses all the claimed subject matter, note 1) the claimed wherein the write address generator, comprises: a first write address generator generating first write addresses associated with a first of the two consecutive scan lines based on the count values is met by the line counter 70 (Fig. 3, col. 4, lines 5-43), 2) the claimed a second write address generator generating second write addresses associated with a second of the two consecutive scan lines based on the count values is met by the write counter 50 (Fig. 3, col. 4, lines 5-43), and 3) the claimed a write address controller selectively outputting one of the first and second write addresses based on whether the progressive scan data is being converted into one of an odd and even scan line of interlaced scan data is met by the line control circuit 72 which issues line/start signals for only those lines, i.e., odd or even (Figs. 3-4, col. 6, line 50 to col. 8, line 53).

In considering claim 23, the claimed wherein the write address controller receives a control signal indicating whether the progressive scan data is being converted into one of an odd and even scan line of interlaced scan data is met by the line control circuit 72 which issues line/start signals for only those lines, i.e., odd or even (Figs. 3-4, col. 6, line 50 to col. 8, line 53).

In considering claim 24, the claimed wherein the read address generator converts the count values into read addresses associated with one scan line of interlaced scan data is met by the read counter 54 (Figs. 3 and 4, col. 4, line 5 to col. 6, line 48).

Claim 25 is rejected for the same reason as discussed in claims 16 and 21 above.

Claim 28 is rejected for the same reason as discussed in claims 16 and 17 above.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4, 15 and 26-27 are rejected under 35 U.S.C. 102(e) as being anticipate by Yugami et al. (US Patent No. 6,927,801 B2).

In considering claim 1, Yugami et al discloses all the claimed subject matter, note 1) the claimed a first converter converting input interlaced scan data into progressive scan data is met by the I-P converter section 1 (Fig. 1, col. 5, line 32 to col. 6, line 18),

and 2) the claimed a second converter converting the progressive scan data output from the first converter to interlaced scan data is met by the P-I conversion section 3 (Fig. 1, col. 7, line 64 to col. 8, line 8).

In considering claim 4, the claimed wherein the second converter converts the progressive scan data output from the first converter to interlaced scan data such that the interlaced scan data output by the second converter is synchronized with the progressive scan data output from the first converter is met by the P-I conversion section 3 which convert 1440P video to 1440i video (Fig. 1, col. 7, line 64 to col. 8, line 8).

Claim 15 is rejected for the same reason as discussed in claim 1 above.

Claim 26 is rejected for the same reason as discussed in claim 1 above.

Claim 27 is rejected for the same reason as discussed in claim 4 above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5-7 and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yugami et al. (US Patent No. 6,927,801 B2) in view of Peterson et al. (US Patent No. 4,386,367).

In considering claim 5, Yugami et al disclose all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the second converter comprises: a counter generating count values at a progressive scanning frequency such that the count values are associated with a period of the progressive scan data; a memory; a write address generator generating write addresses for writing progressive scan data into the memory based on output of the counter; and a generating read addresses for outputting the progressive scan data written into the memory as interlaced scan data based on output of the counter.

Peterson et al teach that the P-I converter which has the control section of the system of FIG. 3, extending across the lower two-thirds of the figure, includes a write counter 50 and write control circuit 52 for control information storage in synchrony with a first clock signal TDCLK, a read counter 54 and the read control circuit 56 for controlling information retrievel in synchrony with a second clock signal XDCLK, ... the storage device 36, the line counter 70 and line control circuit 72... (Figs. 3-4, col. 4, line 5 to col. 6, line 48).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the P-I converter as taught by Peterson et al into Yugami et al's system in order to provide an improved system and method for converting successive frames of a non-interlaced video signal into successive fields of an interlaced signal.

In considering claim 6, the claimed wherein the second converter further comprises: an address controller selectively applying the write and read addresses to

the memory from the write and read address generators is met by the address MUX 58 which is switching alternately between the write address and the read address (Figs. 3 and 4, col. 4, line 5 to col. 6, line 48 of Peterson et al).

In considering claim 7, the claimed wherein the address controller controls the application of the write and read addresses to the memory such that a scan line of interlaced scan data is read from the memory while progressive scan data for the scan line is written to the memory is met by the address MUX 58 which is switching alternately between the write address and the read address (Figs. 3 and 4, col. 4, line 5 to col. 6, line 48 of Peterson et al).

In considering claim 10, the claimed wherein the counter generates count values associated with two consecutive scan lines of progressive scan data is met by the line counter 70 (Fig. 3, col. 4, lines 5-43 of Peterson et al).

In considering claim 11, Peterson et al discloses all the claimed subject matter, note 1) the claimed wherein the write address generator, comprises: a first write address generator generating first write addresses associated with a first of the two consecutive scan lines based on the count values is met by the line counter 70 (Fig. 3, col. 4, lines 5-43), 2) the claimed a second write address generator generating second write addresses associated with a second of the two consecutive scan lines based on the count values is met by the write counter 50 (Fig. 3, col. 4, lines 5-43), and 3) the claimed a write address controller selectively outputting one of the first and second write addresses based on whether the progressive scan data is being converted into one of an odd and even scan line of interlaced scan data is met by the line control circuit 72

which issues line/start signals for only those lines, i.e., odd or even (Figs. 3-4, col. 6, line 50 to col. 8, line 53).

In considering claim 12, the claimed wherein the write address controller receives a control signal indicating whether the progressive scan data is being converted into one of an odd and even scan line of interlaced scan data is met by the line control circuit 72 which issues line/start signals for only those lines, i.e., odd or even (Figs. 3-4, col. 6, line 50 to col. 8, line 53 of Peterson et al).

In considering claim 13, the claimed wherein the read address generator converts the count values into read addresses associated with one scan line of interlaced scan data is met by the read counter 54 (Figs. 3 and 4, col. 4, line 5 to col. 6, line 48 of Peterson et al).

Claim 14 is rejected for the same reason as discussed in claims 5 and 10 above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kondo et al. (US Patent No. 7,012,648 B2) disclose image conversion method and image conversion apparatus.

Lin et al. (US Patent No. 5,912,711) disclose apparatus for converting and scaling non-interlaced VGA signal to interlaced TV signal.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (571) 272-7358. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 11, 2007

Trang U. Tran
Primary Examiner
Art Unit 2622